Power Converter with Signal Frequency and Amplitude Regulation

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Abstract—The paper considers the structure and methods of creating powerful power converters with adjustable output parameters. To change the rotational speed of the shaft of an asynchronous engine (AM/E), the method of amplitude modulation is proposed. To change the engine torque, a method is used to change the capacitance of the capacitor of the converter. As a result, the circuits load voltage changes. The proposed solution based on the method of amplitude modulation with the use of powerful transistor converters makes it possible to amplify a sufficiently weak harmonic input signal (not more than 1.5 W) to tens and hundreds of kilowatts. The use of a two-unit oscillating circuit with a series and parallel capacitors as part of the power converter allows obtaining an undistorted sinusoidal voltage at the output with amplitude and frequency adjustment. Digital control of key elements of the converter allows formalizing the task of monitoring and diagnostics of the electric drive, including remote.

Keywords—power converter; amplitude-modulated signal; replacement circuit; resonant voltage converters

I. INTRODUCTION

At automation of technological processes as a part of executive devices in which basic electric motors are used, it is often necessary to change output parameters of the electric drive (for example, speed of rotation of a shaft and its moment). In addition, many electric drives, when powered by a distorted industrial network, reduce such technical characteristics as power, life time, and etc. The power electronics converters are the part of electric drives. The power electronics converter (PEC) provides the required characteristics. In this paper methods are shown for adjusting the amplitude and frequency of the output undistorted sinusoidal voltage of the PEC. To control asynchronous engine (AE), methods can be applied when the envelope of a low-frequency sinusoid “carries” full information, and a high-frequency sinusoid serves to transmit this signal throughout the entire path, from the control system to the actuator. One method is the amplitude modulation (AM) method. This technique, well developed and described in the technical literature [11] - [13] can be used to create devices with output adjustable parameters - the voltage amplitude and its frequency as a PEC for powering the drive. When forming a powerful AM signal with adjustable frequency, a modern element base is used - powerful MOSFET and IGBT transistors [14], [15]. This makes it possible to simplify the circuit of electric drives and to reduce the weight and size parameters of the drive.

The paper is as follows. Section 2 presents an overview of the amplitude modulated signal method. Section 3 discusses the device implementation, discusses the features of the structure and algorithms of the solved problem of the PEC. Case study of the replacement circuit of the PEC and their discussion are given in Section 4. Section 5 presents discrete method of regulation output parameters. Finally, the conclusion is given in Section 6.

II. THE METHOD OF AMPLITUDE MODULATION

Let us briefly consider the block diagram (Fig. 1) of the amplitude modulator model [3]. The following signals and parameters are indicated in this figure:

1. \( \lambda(t) \) - signal supplied to the input of the AM modulator;
2. \( s(t) \) - carrier-frequency signal \((\omega_0)\);
3. \( \phi_0 \) - initial phase of the input signal \((\phi_0=0)\);
4. \( m_{AM} \) - modulation factor;
5. \( s(\lambda,t) \) - output.

The first modulator input is supplied with a useful signal of arbitrary form, and on the second - a harmonic signal of a higher frequency (carrier). For modeling the modulator, we can change the input parameters \( \phi_0 \) and \( m_{AM} \). If it is necessary, the signal coming from the modulator output can be supplied
to the demodulator and get a copy of the input higher power signal.

As a result of pairwise-cross switching of transistors 2 and 4 (block 6) is leading to the unit 7. Unit 7 is synchronized from the block 6. Thus, the switching on and locking of transistors 2, 5 occur simultaneously. In the other half of the period of current oscillations in the diagonal of the alternating voltage, switching of transistors 3, 4 also occurs simultaneously.

As a result of pairwise-switching of transistors in the bridge arms at the input of a resonant oscillatory system with a load of 9, there arises a 2-polar, rectangular-shaped voltage. The first harmonic of this rectangular voltage appears with the help of the resonant LC-circuit.

To obtain a modulated sinusoid in load 9, it is necessary to introduce into the circuit a block 8 which together with the control unit 7 provides the unlocking of transistors 3 and 5. The carrier frequency is many times greater than the frequency of the modulating voltage 8 source. Thus, slowly varying modulating voltage is superimposed to the pulses of the carrier frequency control signals. When this voltage is increased, the duration of current flow in transistors 3 and 5 decreases, that leads to a decrease of a sinusoidal voltage in the load. This ensures non-simultaneous unlocking of transistors 3 and 5 with respect to transistors 2 and 4.

### III. POWER ELECTRONICS CONVERTER

To generate powerful AM signals, PECs are used, performed on key elements [5]. Figure 2 shows a simplified PC structural circuit for obtaining powerful AM signals. It consists of a power supply 1, key power transistors 2-5, a first control unit (CU) 6 of transistors 2, 4 and a second CU 7 of transistors 3, 5; source of the modulating voltage (low frequency signal) 8, oscillatory system (resonant LC circuit) and load 9.

Transistors 2, 5 are connected according to the transistor bridge scheme. Transistors 2, 4 and 3, 5 are respectively left

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**Fig. 1.** Amplitude Modulator model

**Fig. 2.** PEC structural and functional diagram
For PEC output voltage regulation at a given level it is necessary to add into the circuit an extra capacitor \( C_{add} \), connected in series with the throttle. In this case, to regulate the voltage it is necessary to change its capacitance [10]. To confirm this, the process simulation is carried out. Figure 5 shows the parametric dependences when the \( C_{add} \) capacitance is changed.

IV. CASE STUDY OF THE REPLACEMENT CIRCUIT OF THE POWER ELECTRONICS CONVERTER

To study the power converter operation, a PEC simulation was carried out. For this, a replacement circuit was developed, shown in Fig.3. This scheme includes the following items:

- stabilized power supply \( E \);
- bridge from transistors M1-M4;
- control unit CU of these transistors (U1-U4);
- series-parallel oscillatory circuit, consisting of two contours K1 and K2, which includes a common throttle \( L \), a series load \( RL \) of the capacitor \( C1 \) and a parallel capacitor \( C2 \);
- \( R0 \) is the internal resistance of the power supply \( E \), and \( R5 \) is the inductance resistance \( L \);
- load \( RL \).

To account for losses in the simulation, two resistors are introduced: the internal resistance of the power supply \( E \) and the active resistance of the throttle \( L \). Transistor bridge and filter based on two oscillatory circuits is a serial-parallel inverter.

The device works as follows. Constant stable voltage is applied to one bridge diagonal of four transistors M1-M4. The gate of these transistors is fed with control signals from the CU. In pairwise cross switching of transistors M1, M4 and M2, M3 on the other bridge diagonal, an alternating voltage of rectangular shape arises.

The voltage amplitude is equal to the voltage of the power supply \( E \), which arrives at the input of the filter \( L1, C1, C2 \). This filter is formed by two interconnected resonant circuits, so that the rectangular voltage is converted into a harmonic signal. The process is described in detail in [9],[16],[17].

To study the operation modes of the PEC replacement circuit, mathematical modeling on a computer was carried out. Herewith the features of the filter construction were considered, namely, a series resonance circuit \( L1, C1, RL \) (K1) and parallel \( L1, C2, RL \) (K2). Initially, these circuits are tuned to the resonance frequency necessary to execute the technological process. In PEC design this resonance frequency is specified along with other PEC parameters presented below.

- \( f_R \) - resonant circuit frequency;
- \( U_{Lm} \) – output harmonic voltage amplitude on the load;
- \( P_{Lm} \) - maximum power in load.

To obtain the greatest oscillation amplitude of the PEC output, it is necessary to observe the equality of the frequencies of mechanical and electrical oscillations. Based on the given parameters, it is possible to determine the active resistance of the load \( R_L \), the wave resistance of the contours \( Z_{w1}, Z_{w2} \) and the frequency of their resonance \( f_R \):

\[
R_L = \frac{U_{Lm}^2}{P_{Lm}}
\]

\[
Z_{w1} = \frac{L}{\sqrt{C_1}}, Z_{w2} = \sqrt{\frac{L}{C_2}}
\]
monic will be \( f_{R} \). To get 18, the output frequency of the ular voltage is applied to the  e for the specified characteristics of the -), the subtrahend sulation is carried out. Fig. 5 uture of the power -Larametric dependences when the -control the harmonic requency of 50 Hz to E ary to change its capacitance [10

\[
 f_{R} = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \tag{6}
\]

It should be noted that to use high Q-factor loads, in expression (6), the subtrahend \( \frac{R^2}{4L^2} \) can be neglected. In expression (6), \( R \) is the loss resistance in the circuit.

The Fig.4 shows the time diagrams of the rectangular voltage at the circuit input and the sinusoidal voltage on the load. It is seen that at those instants of time when the currents pulses of the left and right bridge arms begin to gradually be subtracted and, being in anti phase, compensate each other. This process leads to LC circuit state when the input voltage is zero. Further, under the influence of the modulating signal, the voltage at the input of the circuit again increases.

As noted above, if a rectangular voltage is applied to the input of a resonant LC circuit, then its first harmonic will be released on load \( R_{L} \), and the longer the duration of a rectangular pulse, the greater the amplitude of the extracted voltage harmonic on the load. Thus, in load \( R_{L} \), the voltage will have the sinusoidal form with frequency \( f \), but it will be “composed” of the harmonics of the carrier frequency \( f_{c} \).

To study the PEC replacement circuit, we set: the voltage of the power supply \( E = 100 \) V, the output frequency of the sinusoidal signal \( f_{R} = 25 \) kHz, the wave resistance of the oscillating circuit \( Z_{o} = 50 \) Ohm. Thus, using the procedure for calculating the PEC given in [5] and expressions (4) - (6), we can determine the parameters of the oscillatory circuits. The simulation is performed on powerful MOSFET transistors of the type IRFP460 [18].

V. THE PEC OUTPUT PARAMETERS REGULATION

In articles [18] and [19], [20] methods for adjusting the parameters of the PEC are discussed. In article [18], a phase method for adjusting the voltage of the PEC is proposed. The disadvantage of this method is the “dead time” of the operation of key transistors. A resonant voltage converter and ways of pulse width (PWM) adjustment of its output voltage are proposed in the paper [19], [20].

The frequency regulation of the PEC implementation can be carried out in a discrete (digital) way. The discrete method of regulation is setting the set value of the PEC output voltage frequency in the block 8 (Fig.3). To control the harmonic output signal, it is proposed to use the control of the key modulator devices (for example, high-power transistors) with the use of rectangular pulses applied to different bridge arms with various frequencies. For example (see Fig. 3), if control unit CU (U1, U3) apply pulses with a frequency of 50 Hz to transistors M1 - M3 and CU (U2, U4) apply pulses with a frequency of 51 Hz to transistors M2 - M4, then the oscillatory circuit will allocate on the load a harmonic of frequency 1 Hz, filled with a voltage with a carrier frequency.

As noted above, for PEC output voltage regulation at a given level it is necessary to add into the circuit an extra capacitor \( C_{add} \) (see Fig.2) or C1 (in replacement circuit Fig.3 ) connected in series with the throttle. In this case, to regulate the voltage it is necessary to change its capacitance [10]. To confirm this, the process simulation is carried out. Fig. 5 shows the parametric dependences when the C1 capacitor capacitance is changed. As the capacity of the capacitor increases, the maximum voltage and the average value of the power on the load increase, with the voltage of the power supply PEC remaining unchanged. From the graph of Fig. 5 it can be seen that when the capacity of the capacitor is increased 14 times, the voltage on the load (curve 2) increases from 30 V to almost 500 V.

The choice of the control architecture of the power converter is determined by the specified characteristics of the converter operation, the number and quality of the PEC parameters adjustments.

Currently, there are two main approaches to the development of the architecture of the JV management system. First, it is a traditional architecture using a calculator (microprocessor), built on the basis of the von Neumann model [21], which in the literature is called control flow. The main drawback of this model, in terms of speed, is the sequential execution of commands that implement the algorithm. Secondly, the implementation of the management architecture based on the data flow model proposed by D. Dennis, for example [22]. In this case, the implemented algorithm is "sewn up" in the control system equipment in the form of required computing and logical operators, which
allows parallelizing various processes and unlimitedly scaling [5].

The drawback of the data flow model until recently remained the implementation of an efficient, but highly specialized task [23]. When changing the algorithm of the problem, it was necessary to upgrade the hardware part of the control system. With the development of technology field-programmable gate array (FPGA) the situation has changed dramatically. There was an opportunity to reconfigure the hardware implementation of the algorithm an unlimited number of times (and for modern FPGAs even "on the fly"). In addition, the development can be performed in the languages of the hardware description (System Verilog [24], VHDL [25]), which increased the development productivity and made it possible to perform functional and temporary simulation of the project.

Modern FPGAs in their composition contain tools for the effective implementation of the data flow calculation model - digital signal processors (DSPs) that allow the development and implementation of high-performance power converter control loops. For example, Altera developed the Motor Control Development Framework [24], which supports the development of control loops for engine-based motor control in MATLAB / Simulink [25]. This software allows you to reach a new level of system integration, scalability and flexibility when developing applications with very intensive digital processing.

VI. CONCLUSION

In the proposed PEC circuit implementation, a two-unit filter is used: L and C is the filter sequential element, and L and C are a parallel element. This circuit configuration makes it possible to obtain a pure sinusoid, since the load voltage is determined by the oscillating circuit LC [26].

A method is proposed for regulation the powerful PEC frequency based on separating the frequency difference on a two-unit filter using control pulses applied to the bridge shoulders with various frequencies. To the regulation the PC output voltage amplitude in the filter, an additional capacitor with variable capacitance is used.

The power electronics converter can be used as an efficient power supply adjustable over a wide range or a generator of harmonic oscillations with amplitude modulation.

References


[27] https://www.mathworks.com/products/simulink.html